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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,638	09/14/2001	Christophe Lauga	851963.401	6890

500 7590 01/14/2004

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/954,638	LAUGA, CHRISTOPHE	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 8-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ayres et al. (US 6263461).

Regarding independent Claims 1 and 10, Ayres discloses a circuit for efficiently testing memory and shadow logic of a semiconductor integrated circuit, including a plurality of combinational logic components (101), a memory (120) and a testing arrangement BIST circuitry (201, 202, 203 and 204) for configuring the memory prior to testing the combinational logic components using one or more scan chains, the arrangement, Figure 3, comprising:

A data generator (301, Figure 3) for generating a predetermined bit pattern test data (Test Din) based on input from an external built in test controller for writing to the memory block (120).

A switching arrangement (multiplexers 302, 304) for selectively switching the memory input (120, Din), for receiving data from the combinational logic components input shadow (101) or from the data generator (301).

Wherein the switching arrangement (multiplexer 302) and data generator (301) are arranged to input the predetermined bit pattern to the memory (120) prior to testing the integrated circuit, by writing the test data into memory block 120, described in step 405, Figure 4A.

Regarding Claim 2, Ayres discloses testing arrangement BIST circuitry (201, 202, 203 and 204), where the control interface 203 receives normal control signals from input shadow 101 indicating whether the pending operation is a read or write, by sending test control signals to the memory block 120 via multiplexer 305.

Regarding Claims 3 and 13, Ayres discloses bit pattern data generator (301, Figure 3) for a given address comprising a function of the address bit sequence (address generator 303) for presenting the bit pattern at outputs corresponding to address inputs (ADDR) of the memory (120).

Regarding Claims 4 and 11, Ayres discloses an arrangement of multiplexers (302, 304) to selectively connect the memory (120) to the combinational logic components (101), or to the data generator (301).

Regarding Claims 5 and 15, Ayres discloses an address generator (303) for generating addresses to write the bit pattern in the memory (120) from the data generator (301) including interconnections (ADDR lines) coupling the output of multiplexer (304) with the memory ADDR (120).

Regarding Claim 8, Ayres discloses a wrapper circuit (Test collar 110) coupled between the memory block (120) and shadow logic (101) for connecting the memory to other components in the integrated circuit.

Regarding Claims 9 and 19, Ayres discloses a wrapper controlling the memory to behave as a ROM, since no data is read out during the WRITE cycle.

Regarding Claims 12 and 14, Ayres discloses data generator (301, Figure 3) for generating a selected predetermined bit pattern test data (Test Din) based on input from an external built in test controller for writing to the memory block (120), prior to testing.

Regarding Claims 16, 17 and 18, Ayres discloses pattern data generator (301, Figure 3) for writing in specific memory array comprising DRAM, SRAM (column 7, line 5-14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ayres et al. (US 6263461) in view of Rapoport (US 5557619).

Regarding Claims 6 and 7, Ayres does not disclose a checkerboard pattern in the memory and wherein the pattern is so arranged that the RAM may be modeled as a simple combinational circuit.

However, Rapoport discloses a novel processor-based ABIST circuit, which can be programmed with a "read complement checkerboard pattern", to verify the functionality of memory unit 12. In addition he discloses conventional state machine based ABIST having combinational logic circuits to generate each hard-coded test pattern, (column 11, line 30-35). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the ABIST 20 having a checkerboard pattern and combinational logic circuits, as taught by Rapoport, for generating the necessary bit pattern to verify the functionality of a RAM memory in the apparatus of Ayres, since the test patterns that are generated with the conventional state machine based ABIST units are still available, as well as an assortment of new programmable test patterns, thus providing design flexibility.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4900.

James C Kerveros
Examiner
Art Unit 2133

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
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Date: 9/01/2004
File: Non-Final Rejection

By:

Guy J. Lamare
for
Albert DeCady
Primary Examiner